REMARKS

Claims 1-10 are presented for examination. It is noted that the Office Action contains an error because it indicates on page 2 that claims 1-14 have been cancelled.

Claims 1-10 have been rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

It is respectfully submitted that this rejection is defective. The Office action contains two different and contradictory rejections of claims 1-10 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Some language of these rejections coincides but some phrases are different. It is not clear which one of these rejections was supposed to be included in the Office Action.

However, to comply with the Examiner's request, claim 1 has been amended to more clearly define the claimed invention. In particular, the amended claim recites that said data operation unit executes data transfer between registers and data transfer between one of said registers and said memory in correspondence to single said instruction code having a single operation code fetched by said program control unit.

Further, it is noted that the Examiner takes the position that the "Applicant's specification, page 12, lines 3-12 and fig. 9A taught a single instruction code POP instruction with two operational codes (pop(1) with no register and pop(2) with a register as shown in fig. 9A)."

This Examiner's position is respectfully traversed for the following reasons.

Applicant respectfully submits that each of "pop" and "pop ra" in fig. 9A is a single instruction code and has only a single operation code.

Moreover, the specification on page 12, lines 3-12 does not disclose a single instruction code POP instruction with two operational codes. Instead, the specification discloses two scenarios. One relates to the case when the POP instruction specifies no register, and another – relates to the case when the POP instruction specifies a register.

Accordingly, neither the specification nor fig. 9A provides support for the Examiner's position that a single instruction code POP has two operational codes. Therefore, the Examiner's position is unwarranted.

Claims 1-10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Col et al. in view of Volentine et al.

This rejection is respectfully traversed for the following reasons.

Claim 1 recites a microprocessor including:

a program control unit controlling fetch of an instruction code;

an instruction decode unit decoding said fetched instruction code;

an address operation unit operating an address of a memory on the basis of the result of decoding by said instruction decode unit; and

a data operation unit operating data on the basis of the result of decoding by said instruction decode unit, wherein

said data operation unit executes data transfer between registers and data transfer between one of said registers and said memory in correspondence to single said instruction code having a single operation code fetched by said program control unit.

The Examiner admits that Col does not disclose the data transfer between registers, as claim 1 requires.

Volentine is relied upon for disclosing this feature.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

The claimed invention requires two data transfer operations, one of which is data transfer between registers and another - is data transfer between one of the registers and the memory, in correspondence to a single instruction code having a single operation code.

Hence, the invention requires both data transfers to be performed in correspondence to the same instruction code.

However, even assuming *arguendo* that Col was modified in view of Volentine, the claimed invention would not result.

In particular, Col discloses a data transfer between registers and memory in response to one instruction code, and Volentine suggests a data transfer between registers in response to another instruction code.

Therefore, a combination of Col with Volentine would suggest a data transfer between registers and memory in response to one instruction code, and a data transfer between registers in response to another instruction code.

Accordingly, the combined teachings of the references are not sufficient to arrive at the claimed invention requiring data transfer between registers and data transfer between one of the registers and the memory in correspondence to a single instruction code having a single operation code.

The Examiner has apparently failed to give adequate consideration to the particular problems and solution addressed by the claimed invention. ***Northern Telecom, Inc. v. Datapoint Corp.***, 908 F.2d 931, 15 USPQ2d 1321 (Fed. Cir. 1990); ***In re Rothermel***, 276 F.2d 393, 125 USPQ 328 (CCPA 1960). Specifically, none of the references addresses performing data transfer between registers and data transfer between one of the registers and the memory in correspondence to the same instruction code having a single operation code.

Hence, the Examiner's position of obviousness is not warranted. Applicant, therefore, respectfully submits that the rejection of claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over Col et al. in view of Volentine et al. is improper and should be withdrawn.

Claims 1-10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Mandavilli in view of Morrison et al.

The Examiner admits that Mandavilli does not disclose the data transfer between register and memory, as claim 1 requires.

Morrison is relied upon for disclosing this feature.

Similarly to the previous rejection, even assuming *arguendo* that Mandavilli were modified in view of Morrison, the claimed invention would not result.

In particular, Morrison discloses a data transfer between a register and memory in response to one instruction code, and Mandavilli suggests a data transfer between registers in response to another instruction code.

Therefore, a combination of Mandavilli with Morrison would suggest a data transfer between registers and memory in response to one instruction code, and a data transfer between registers in response to another instruction code.

Accordingly, the combined teachings of the references are not sufficient to arrive at the claimed invention requiring data transfer between registers and data transfer between one of the registers and the memory in correspondence to a single instruction code having a single operation code.

Hence, the Examiner's position of obviousness is not warranted. Applicant, therefore, respectfully submits that the rejection of claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over Mandavilli in view of Morrison et al. is improper and should be withdrawn.

In view of the foregoing, and in summary, claims 1-10 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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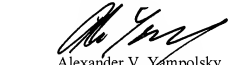

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